WHAT IS CLAIMED IS:

1. A method for generating a delay signal, comprising steps of:

providing a plurality of source signals, every adjacent two of which have a phase difference of a certain clock unit;

generating a first and a second output signals at a first and a second time points based on said plurality of source signals; and

processing said first and said second output signals by a logic operation to obtain said delay signal.

2. The method according to claim 1, wherein said plurality of source signals are generated from a high-frequency signal by a phase-locked loop (PLL) device.

3. The method according to claim 1, wherein said plurality of source signals are a series of increasingly lagging signals.

4. The method according to claim 1, wherein said plurality of source signals are a series of increasingly leading signals.

5. The method according to claim 1, wherein said logic operation is an XOR operation.

6. The method according to claim 1, wherein said step of generating said first and said second output signals comprises sub-steps of:

deriving a first and a second signal groups from said plurality of source signals;

selecting a signal from said first signal group at said first time point as said first output signal; and

selecting a signal from said second signal group at said second time point as said second output signal.

7. The method according to claim 6, wherein said first and said second signal groups are obtained by duplicating said plurality of source signals.

8. The method according to claim 6, wherein said first and said second time points are predetermined, and located by counting operations in response to a first and a second clock signals, respectively.
9. The method according to claim 1, wherein said first output signal is generated based on the same first edges of selected two of said plurality of source signals, and said second output signal is generated based on the same second edges of selected two of said plurality of source signals.
10. The method according to claim 9, wherein said first and said second edges are both rising edges.
11. The method according to claim 9, wherein a delay period of said delay signal is determined by the same third edges of said first and said second output signals.
12. The method according to claim 11, wherein said third edges are rising edges or falling edges.
13. The method according to claim 6, wherein said first and said second signal groups are divided into a first and a second plurality of signal sub-groups, and said first and said second output signals are generated from one of said first plurality of signal sub-groups and one of said second plurality of signal sub-groups, respectively.
14. The method according to claim 13, wherein all source signals in the selected one of said first plurality of signal sub-groups are at the same first level at said first time point, and all source signals in the selected one of said second plurality of signal sub-groups are at the same second level at said second time point.
15. The method according to claim 14, wherein said first and said second levels are both low levels.

16. A device for generating a delay signal, comprising:

a source-signal generator generating and outputting N counts of source signals in response to a high frequency signal, every adjacent two of said N counts of source signals having a phase difference of a certain clock unit;

a source-signal selector coupled to said source-signal generator, and selecting a first and a second ones of said N counts of source signals to be outputted at a first and a second time points in response to a first and a second clock signals as a first and a second output signals, respectively, and

a logic operator coupled to said source-signal selector, and logically operating said first and said second output signals to obtain said delay signal.

17. The device according to claim 16, wherein said source-signal generator is a phase-locked loop (PLL) device.

18. The device according to claim 16, wherein said source-signal selector includes:

a selection-signal generating circuit generating a first and a second selection signal sets in response to said N counts of source signals and said first and said second clock signals;

a first multiplexing circuit coupled to said selection-signal generating circuit, and allowing said first one of said N counts of source signals to be outputted as said first output signal in response to said first selection signal; and

a second multiplexing circuit coupled to said selection-signal generating circuit, and allowing said second one of said N counts of source signals to be outputted as said second output signal in response to said second selection signal.

19. The device according to claim 18, wherein said first multiplexing circuit includes M1 counts of multiplexers receiving different portions of said N counts of source signals, respectively, and allowing M1 ones among said N

counts of source signals to be outputted as M1 counts of multiplexing output signals in response to M1 counts of selection signals included in said first selection signal set, and said second multiplexing circuit includes M2 counts of multiplexers for receiving different portions of said N counts of source signals, respectively, and allowing M2 ones among said N counts of source signals to be outputted as M2 counts of multiplexing output signals in response to M2 counts of selection signals included in said second selection signal set.

20. The device according to claim 19, wherein said source-signal selector further includes:

a first signal synthesizing circuit coupled to said first multiplexing circuit for synthesizing said M1 counts of multiplexing output signals into said first output signal; and

a second signal synthesizing circuit coupled to said second multiplexing circuit for synthesizing said M2 counts of multiplexing output signals into said second output signal.

21. The device according to claim 20, wherein each of said first and said second signal synthesizing circuits includes an OR gate.

22. The device according to claim 20, wherein said first signal synthesizing circuit includes:

M1 counts of AND gates coupled to said selection-signal generating circuit, said M1 counts of multiplexers and said source-signal generator, performing an AND operation of M1 counts of decoding signals, said M1 counts of multiplexing output signals and M1 counts of specific signals, and outputting M1 counts of gate output signals, respectively; and

a first OR gate coupled to said M1 counts of AND gates, and performing a

first OR operation of said M1 counts of gate output signals to obtain said first output signal, and

said second signal synthesizing circuit includes:

M2 counts of AND gates coupled to said selection-signal generating circuit, said M2 counts of multiplexers and said source-signal generator, performing an AND operation of M2 counts of decoding signals, said M2 counts of multiplexing output signals and M2 counts of specific signals, and outputting M2 counts of gate output signals, respectively; and

a second OR gate coupled to said M2 counts of AND gates, and performing a second OR operation of said M2 counts of gate output signals to obtain said second output signal.

23. The device according to claim 22, wherein each of said M1 counts of specific signals is identical to one of said source signals, and kept at least P counts of clock cycles of said first clock signal leading or lagging all said source signals inputted into the corresponding multiplexer, and each of said M2 counts of specific signals is identical to one of said source signals, and kept at least P counts of clock cycles of said second clock signal leading or lagging all said source signals inputted into the corresponding multiplexer.

24. The device according to claim 23, wherein the number N, M1, M2 and P are 32, 4, 4, and 4, respectively.

25. The device according to claim 16, wherein said selection-signal generating circuit comprises:

a first selection signal decoder generating said M1 counts of decoding signals in response to said first clock signal;

M1 counts of operating units, each coupled to said first selection signal decoder and outputting an output control signal in response to one of said M1

counts of decoding signals and (N/M1) ones of said N counts of source signals;

M1 counts of output units, each coupled to said first selection signal decoder and one of said M1 counts of operating units, and outputting one of said M1 counts of selection signals in response to said first clock signal, one of said M1 counts of decoding signals and one of said M1 counts of output control signals;

a second selection signal decoder generating said M2 counts of decoding signals in response to said second clock signal;

M2 counts of operating units, each coupled to said second selection signal decoder and outputting an output control signal in response to one of said M2 counts of decoding signals and (N/M2) ones of said N counts of source signals;

M2 counts of output units, each coupled to said second selection signal decoder and one of said M2 counts of operating units, and outputting one of said M2 counts of selection signals in response to said second clock signal, one of said M2 counts of decoding signals and one of said M2 counts of output control signals;

26. The device according to claim 25, wherein each of said M1 counts of operating units is an OR gate for performing an OR operation of said (N/M1) ones of said N counts of source signals, and each of said M2 counts of operating units is an OR gate for performing an OR operation of said (N/M2) ones of said N counts of source signals.

27. The device according to claim 25, wherein each of said M1 and M2 counts of output units is a transparent latch.

28. The device according to claim 16, wherein said logic operator comprises:

a storage unit for storing therein said first and said second output signals; and

a logic operation unit coupled to said storage unit and logically operating said first and said second output signals to obtain said delay signal.

29. The device according to claim 28, wherein said storage unit includes a first and a second T flip-flops for storing therein said first and said second output signals, respectively.

30. The device according to claim 28, wherein said storage unit includes a first and a second R-S latches for storing therein said first and said second output signals, respectively.

31. The device according to claim 28, wherein said logic operation unit is an XOR gate.